REMARKS

In view of the foregoing amendments and following remarks responsive to the Final Office Action dated October 31, 2007, Applicant respectfully requests favorable reconsideration of this application.

Claims 1, 3, 4, 6, 7, and 9-17, 19, and 20 were pending in this application. Claims 1, 7, 14, and 17 are independent.

Applicant offers no claim amendments herein. Applicant has, however, amended the specification to correct a few obvious typographical errors.

Accordingly, claims 1, 3, 4, 6, 7, and 9-17, 19, and 20 remain pending in this application.

The Office has maintained and made final the rejection of all of the claims as obvious over Gerlach in view of Yamamoto.

Applicant respectfully traverses. Particularly, as argued in the previous response, independent claims 1, 14, and 17 each include a recitation that at least one of the switching topologies includes two cascaded stages and independent claims 7 recites that the switching topologies comprise a plurality of field effect transistors having their current paths coupled in series between an associated transmission port and the antenna port. The term "cascaded" refers to the type of topology illustrated in Figures 2 and 4 of the present application wherein the current path of a first transistor (e.g., transistor 19) (the first cascaded stage) is coupled to the current paths of multiple transistors (e.g., transistors 20 and 22) (the second cascaded stage).

In the specific embodiment described in the specification, for instance, the switch 108 in Figure 5 would be the first stage of a cascaded switch (e.g., transistor 19 of Figure 2) and the switch 118 in Figure 5 would be the second stage of the cascaded switch (e.g., parallel transistors 20, 22, et seq. of Figure 2). As described in the specification, this cascaded topology, as opposed to the series topology of the prior art illustrated by Figure 1, decreases the insertion loss of the switching topology.

In the rejections, the Office relies on Gerlach as teaching the general proposition of a single-die integrated circuit for switching among a plurality of transmission ports and a plurality of receiver ports, but concedes that Gerlach does not disclose cascaded switches. The Office relies on Yamamoto as teaching the cascaded switching topology and asserts that it would have been obvious to combine the respective teachings of Gerlach and Yamamoto.

Ignoring for the moment the issues of (1) whether Gerlach teaches that for which it has been cited and (2) whether the proposed combination is obvious, the rejection suffers from a fundamental flaw insofar as Yamamoto does not teach the cascaded switching arrangement that is the subject of the present invention.

As previously explained in response to the previous Office Action, Yamamoto discloses a cascode amplifier, which is an entirely different thing than the cascade switch of the present invention.

In response to Applicant's previous arguments, in the Response to Arguments section of the final Office Action, the Office argued:

> The Examiner respectfully disagrees because Yamamoto teaches a first transmission arm circuit connected between said first transmitter and said antenna, said first transmission arm circuit including a first switching circuit which is turned on during transmission and is turned off during reception, a second transmission arm circuit connected between said second transmitter and said antenna, said second transmission arm circuit including a second switching circuit, a reception arm circuit connected between said receiver and said antenna, said reception arm circuit including a third switching circuit. Said third switching circuit comprises a plurality of FET's connected in series with one another. First and second transmission arm circuit comprises a cascade amplifier wherein the chip size can be remarkably reduced in the chip obtained by integrating the power amplifier with duplexer circuit, and the insertion loss during transmission can be reduced (Yamamoto et al, - Figure 8, Figure 9, Figure 10, column 3, lines 47-67, and column 4 lines 1-20, column 11, lines 4-51, column 11 lines 61-67, and column 12 lines 33-52).

This explanation clarifies an issue raised by Applicant in the response to the previous Office action insofar as it was unclear which switching circuit the Office believed comprised a cascade switching configuration. Particularly, it clarifies that the Office believes that each of the transmission-side switching

configurations in Yamamoto comprises a cascade switching configuration. Also, it clarifies that the Office considered Figures 8-10 as significant, whereas this was unclear in the previous Office Action.

Applicant respectfully traverses insofar as the transmission-side switching arrangements in Figures 8, 9, and 10 are not cascaded switching arrangements. In the response to the previous Office Action, Applicant described the distinctions of the cascaded switching configuration of the present invention over the transmission-side switching configuration of Yamamoto's Figure 7. Figures 8, 9, and 10 have the same switching configurations as Figure 7 and, therefore, that discussion is entirely applicable to Figures 8, 9, and 10 as well. Specifically, the only differences between the various embodiments of Figures 7, 8, 9, and 10 are outlined below.

Figure 7 – Basic configuration discussed in detail in the response to the previous Office Action;

Figure 8 – Same as Figure 7, but with two transmitters and two transmitter switching configurations identical to each other and to the single transmission-side switching configuration in Figure 7;

Figure 9 – Same as Figure 8, but with slight modification to the receiver-side switching arrangement (which is not relevant since the Office is relying on the transmission-side switching configuration in the rejection);

Figure 10 - Same as Figure 8, but with a different modification to the irrelevant receiver-side switching configuration.

Contrary to the Office's assertions, F_{1a} and F_{2a} or F_{1b} and F_{2b} in Figures 8, 9, and 10 are not cascade coupled transistors, as recited in independent claims 1, 14, and 17, nor are they even coupled with their current paths in series between the transmitter and the transmission node, as recited in independent claim 7.

Specifically, as described with respect to the Figure 7 embodiment of Yamamoto in the response to the previous Office Action, this arrangement is a

cascode amplifier, i.e., comprising a common emitter transistor, F_{1a} or F_{1b}, and a common gate transistor, F_{2a} or F_{2b}.

Since the switching arrangements are identical for each transmitter, we shall discuss the first one, comprising F_{1a} and F_{2b} between transmitter 101a and node 4, as exemplary. This is not a cascaded switch. In fact, two transistors cannot form a cascade. It takes a minimum of three transistors to form a cascade since a cascade involves coupling a current path terminal (e.g., drain or source) of a transistor in the first stage of the cascade to a current path terminal of each of at least two transistors in the last stage of the cascade. Thus, this configuration is not a cascade as claimed in independent claims 1, 14, and 17, but is a cascode amplifier.

The fact that there are two transmission paths to node 4 in the embodiments of Figures 8, 9, and 10 (as opposed to the single path embodiment of Figure 7 discussed I the previous response) does not make any difference. The claims recite that the cascade configuration exists between one port and one node.

Furthermore and in any event, even considering F_{1a}, F_{2a}, F_{1b}, and F_{2b} collectively, there is no rational way that they could be considered to be cascade coupled (or coupled in series) in any event.

Thus, independent claims 1, 14, and 17 clearly distinguish over the prior art of record.

With respect to independent claim 7, these two series transistors, F_{1a}, F_{2a}, are not coupled in series between the transmitter and the antenna, as claimed. The transmitter output is not coupled to one of the current path terminals of transistor F_{1a}, but to its gate. This configuration is not even properly considered a switch. It is an amplifier. Particularly, it is a cascode amplifier. Despite the similarity in the words “cascode” and “cascade”, a cascode amplifier is a completely different animal than a cascaded switch.

Thus, independent claim 7 also clearly distinguishes over the prior art of record.

Perhaps the fact that Yamamoto expressly talks about reducing the insertion loss (as does the present invention) has lead the Office to the improper conclusion that Yamamoto contains teachings similar to that of the present application. However, that is not accurate. Specifically, Yamamoto claims to have reduced insertion loss by developing a configuration that combines the duplexer and amplifier functions (Yamamoto, column 4, lines 13-18), which is simply different than the present invention.

Accordingly, independent claims 1, 7, 14, and 17 clearly patentably distinguish over the prior art of record.

Dependent claims 3, 4, 6, 8-13, 15-17, 19, and 20 distinguish over the prior art for at least all of the reasons as the independent claims from which they depend. However, the dependent claims even further distinguish over the prior art of record.

For instance, dependent claim 4 depends from claim 1 and adds that each transmitter switching section includes a series FET switching topology comprising "a plurality of transistors with their current paths coupled in series between an associated transmission port and the transmission node". As discussed above in connection with claim 7, none of F_1 and F_2, F_{1a} and F_{2a}, and F_{1b} and F_{2b} in the transmitter switching topology of Yamamoto Figures 7-10 are coupled with their current paths (e.g., source to drain path) in series between the transmission port and the transmission node. As previously noted, this is a cascode amplifier configuration in which the transmitter is coupled to the gate terminal of F_{1a}, not to one of its current path terminals. In Yamamoto Figures 7-10, transistors F_{1a} and F_{2a} are coupled with their current paths between ground and node 4.

Dependent claims 6 and 9 depend from independent claims 1 and 7, respectively, and even further distinguish over the prior art of record. They recite that at least one of the FETs has "a plurality of contiguous source regions interdigitated with a plurality of contiguous drain regions, a sinuous gate formed to wind between the source regions and the gate regions". The Office asserts

that this is found in Yamamoto at column 5, lines 57-67, column 6, lines 1-9, and column 11, lines 3-61. However, neither these portions nor any other portions of Yamamoto discuss the physical layout of the transistors, and, thus Yamamoto is entirely irrelevant.

Dependent claim 15 depends from claim 14 and further elaborates on the cascaded transistor configuration and, therefore, even further distinguished over the prior art of record.

Dependent claim 10 depends from independent claim 7 and adds the limitation that the transmitter port switching topologies occupy an area on the die substantially larger than the receiver port switching topologies. The Office asserted that this is found in Yamamoto at column 11, lines 3-23 and 51-67. However, neither these portions nor any other portions of Yamamoto have anything whatsoever to do with the transistors' physical layout. Accordingly, Yamamoto not only does not disclose what is claimed in claim 10, but is entirely irrelevant to claim 10.

In view of the foregoing remarks, this application is now in condition for allowance. Applicant respectfully requests the Office to issue a Notice of Allowance at the earliest possible date. The Examiner is invited to contact Applicant's undersigned counsel by telephone call in order to further the prosecution of this case in any way.

Respectfully submitted,

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